CLAIMS

What is claimed is:

1. A configurable integrated circuit comprises:

at least one general purpose input/output (GPIO) interface module that includes a plurality of GPIO cells, wherein a GPIO cell of the plurality of GPIO cells is operably coupled to a corresponding pin of the configurable integrated circuit, wherein, when the configurable integrated circuit is in a first functional mode, the GPIO cell is operably coupled to the corresponding pin such that the corresponding pin functions as a digital input pin and when the configurable integrated circuit is in a second functional mode, the GPIO cell is operably coupled to the corresponding pin such that the corresponding pin functions as a digital output pin;

a first functional module having a connection operably coupled to the GPIO cell when the configurable integrated circuit is in the first functional mode; and

second functional module having a connection operably coupled to the GPIO cell when the configurable integrated circuit is in the second functional state.

2. The configurable integrated circuit of claim 1 further comprises:

programmable logic fabric operably coupled between the at least one GPIO interface module and the first or second function module.

3. The configuration integrated circuit of claim 2 further comprises:

remaining GPIO cells of the plurality of GPIO cells are operably coupled to the programmable logic fabric, wherein the programmable logic fabric is programmed to provide at least one of:

coupling between at least some of the remaining GPIO cells and corresponding pins of a set of pins of the configurable integrated circuit;

processing of inbound digital signals when the configurable integrated circuit is in the first functional mode; and

processing of outbound digital signals when the configurable integrated circuit is in the second functional mode.

4. The configurable integrated circuit of claim 1, wherein the first function module and second function module comprises at least one of:

a liquid crystal display (LCD) interface module;
a light emitting diode (LED) interface module;
a random access memory (RAM) interface module;
a compact disk (CD) control interface module;
flash memory module;
hard drive;
random access memory (RAM) module;
a two-wire interface module; and
a system packet interface module.

5. The configurable integrated circuit of claim 1, wherein each of the plurality of GPIO cells comprises:

a data input buffer having an input and an output, wherein the input of the data input buffer is operably coupled to the corresponding pin;

a data output buffer having an input and an output, wherein the output of the data output buffer is operably coupled to the corresponding pin;

a data input connection operably coupled to, when enabled, provide an inbound data signal from the output of the data input buffer to the first functional module;

a data input register operably coupled to, when enabled, store the inbound data signal for subsequent access by a processing core;

a data output connection operably coupled to, when enabled, provide an outbound data signal from the second functional module to the input of the data output buffer;

a data output register operably coupled to, when enabled, provide an alternate outbound data signal to the input of the data output buffer; and

an input/output selection module operably coupled to enable at least one of the data input buffer, the data output buffer, the data input connection, the data input register, the data output connection, and the data output register.

6. The configurable integrated circuit of claim 5, wherein the input/output selection module comprises:

a first control register operably coupled to store a multiplexer selection signal;

a second control register operably coupled to store an overwriting enable/disable signal;

a first multiplexer operably coupled to provide the outbound data signal to the input of the data output buffer when the multiplexer selection signal is in a first state and to provide the alternate output data signal to the input of the data output buffer when the multiplexer selection signal is in a second state; and

a second multiplexer operably coupled to provide an output enable signal to the data output buffer when the multiplexer selection signal is in a third state and to provide the overwriting enable/disable signal to the data output buffer when the multiplexer selection signal is in a fourth state.

7. The configurable integrated circuit of claim 6 further comprises:

the multiplexer signal being in the first state and the third state simultaneously, the first state and the fourth state simultaneously, the second state and the third state simultaneously, or the second state and the fourth state simultaneously.

8. The configurable integrated circuit of claim 1, wherein the at least one general purpose input/output (GPIO) interface module further comprises:

a first GPIO interface module operably coupled to the first and second functional modules; and

a second GPIO interface module operably coupled to a third functional module and a fourth functional module, wherein, when the configurable integrated circuit is in a third functional mode, a GPIO cell of the second GPIO interface module is operably coupled to a second corresponding pin such that the second corresponding pin functions as a digital input pin and when the configurable integrated circuit is in a second functional mode, the GPIO cell of the second GPIO interface module is operably coupled to the second corresponding pin such that the second corresponding pin functions as a digital output pin.

9. A configurable general purpose input/output (GPIO) comprises:

a first GPIO cell operably coupled to a first pin of an integrated circuit to receive first input signals from the first pin and provide the first input signals to a first circuit when a mode selection signal is in a first state and to provide the first input signals to a first register when the mode selection signal is in a second state, wherein the first GPIO is further operably coupled to provide first output signals from a second circuit to the first pin when the mode selection signal is in a third state and to provide first alternate output signals from a second register to the first pin when the mode selection signal is in a fourth state; and

a second GPIO cell operably coupled to a second pin of the integrated circuit to receive second input signals from the second pin and provide the second input signals to a third circuit when a second mode selection signal is in a first state and to provide the second input signals to a third register when the second mode selection signal is in a second state, wherein the second GPIO is further operably coupled to provide second output signals from a fourth circuit to the second pin when the second mode selection signal is in a third state and to provide second alternate output signals from a fourth register to the second pin when the second mode selection signal is in a fourth state.

10. The configurable GPIO of claim 9, wherein the first GPIO cell comprises:

a data input buffer having an input and an output, wherein the input of the data input buffer is operably coupled to the first pin;

a data output buffer having an input and an output, wherein the output of the data output buffer is operably coupled to the first pin;

a data input connection operably coupled to, when enabled, provide the first input signals from the output of the data input buffer to the first circuit;

the first register operably coupled to, when enabled, store the first input signals for subsequent access by a processing core;

a data output connection operably coupled to, when enabled, provide the first output signals from the second circuit to the input of the data output buffer;

the second register operably coupled to, when enabled, provide the first alternate output signals to the input of the data output buffer; and

an input/output selection module operably coupled to enable at least one of the data input buffer, the data output buffer, the data input connection, the first register, the data output connection, and the second register.

11. The configurable GPIO of claim 10, wherein the input/output selection module comprises:

a first control register operably coupled to store a multiplexer selection signal;

a second control register operably coupled to store an overwriting enable/disable signal;

a first multiplexer operably coupled to provide the first output signals to the input of the data output buffer when the multiplexer selection signal is in a first state and to provide the first alternate output signals to the input of the data output buffer when the multiplexer selection signal is in a second state; and

a second multiplexer operably coupled to provide an output enable signal to the data output buffer when the multiplexer selection signal is in a third state and to provide the overwriting enable/disable signal to the data output buffer when the multiplexer selection signal is in a fourth state.

12. The configurable GPIO of claim 9, wherein the second GPIO cell comprises:

a data input buffer having an input and an output, wherein the input of the data input buffer is operably coupled to the second pin;

a data output buffer having an input and an output, wherein the output of the data output buffer is operably coupled to the second pin;

a data input connection operably coupled to, when enabled, provide the second input signals from the output of the data input buffer to the third circuit;

the third register operably coupled to, when enabled, store the second input signals for subsequent access by a processing core;

a data output connection operably coupled to, when enabled, provide the second output signals from the fourth circuit to the input of the data output buffer;

the fourth register operably coupled to, when enabled, provide the second alternate output signals to the input of the data output buffer; and

an input/output selection module operably coupled to enable at least one of the data input buffer, the data output buffer, the data input connection, the first register, the data output connection, and the second register.

13. The configurable GPIO of claim 12, wherein the input/output selection module comprises:

a first control register operably coupled to store a multiplexer selection signal;

a second control register operably coupled to store an overwriting enable/disable signal;

a first multiplexer operably coupled to provide the second output signals to the input of the data output buffer when the multiplexer selection signal is in a first state and to provide the second alternate output signals to the input of the data output buffer when the multiplexer selection signal is in a second state; and

a second multiplexer operably coupled to provide an output enable signal to the data output buffer when the multiplexer selection signal is in a third state and to provide the overwriting enable/disable signal to the data output buffer when the multiplexer selection signal is in a fourth state.

14. The configurable GPIO of claim 9 further comprises at least one of:

the first circuit and the second circuit being part of a functional module; and

the first and second circuits being part of different functional modules.

15. The configurable GPIO of claim 9 further comprises at least one of:

the third and fourth circuits being part of a functional module; and

the third and fourth circuits being part of different functional modules.

16. A multiple function system on a chip integrated circuit comprises:

a processing module;

on-chip memory operably coupled to the processing module;

memory interface for accessing off-chip memory, wherein at least of the on-chip memory and the off-chip memory store operational instructions that cause the processing module to perform at least one of a data file storage function, audio storage function, and audio playback function;

a plurality of functional modules operably coupled to the processing module; and

at least one general purpose input/output (GPIO) interface module operably coupled to the plurality of functional modules and the processing module, wherein the at least one GPIO includes a plurality of GPIO cells, wherein a GPIO cell of the plurality of GPIO cells is operably coupled to a corresponding pin of the multiple function system of a chip integrated circuit, wherein, when the multiple function system of a chip integrated circuit is in a first functional mode, the GPIO cell is operably coupled to the corresponding pin such that the corresponding pin functions as a digital input pin and when the multiple function system of a chip integrated circuit is in a second functional mode, the GPIO cell is operably coupled to the corresponding pin such that the corresponding pin functions as a digital output pin.

17. The multiple function system on a chip integrated circuit of claim 16 further comprises:

programmable logic fabric operably coupled between the at least one GPIO interface module and at least one of the plurality of function modules.

18. The multiple function system on a chip integrated circuit of claim 17 further comprises:

remaining GPIO cells of the plurality of GPIO cells are operably coupled to the programmable logic fabric, wherein the programmable logic fabric is programmed to provide at least one of:

coupling between at least some of the remaining GPIO cells and corresponding pins of a set of pins of the configurable integrated circuit;

processing of inbound digital signals when the multiple function system of a chip integrated circuit is in the first functional mode; and

processing of outbound digital signals when the multiple function system of a chip integrated circuit is in the second functional mode.

19. The multiple function system on a chip integrated circuit of claim 16, wherein the plurality of function modules two or more of:

a liquid crystal display (LCD) interface module;
a light emitting diode (LED) interface module;
a random access memory (RAM) interface module;
a compact disk (CD) control interface module;
flash memory interface module;
hard drive;
a two-wire interface module; and
a system packet interface module.

20. The multiple function system on a chip integrated circuit of claim 16, wherein each of the plurality of GPIO cells comprises:

a data input buffer having an input and an output, wherein the input of the data input buffer is operably coupled to the corresponding pin;

a data output buffer having an input and an output, wherein the output of the data output buffer is operably coupled to the corresponding pin;

a data input connection operably coupled to, when enabled, provide an inbound data signal from the output of the data input buffer to the first functional module;

a data input register operably coupled to, when enabled, store the inbound data signal for subsequent access by a processing core;

a data output connection operably coupled to, when enabled, provide an outbound data signal from the second functional module to the input of the data output buffer;

a data output register operably coupled to, when enabled, provide an alternate outbound data signal to the input of the data output buffer; and

an input/output selection module operably coupled to enable at least one of the data input buffer, the data output buffer, the data input connection, the data input register, the data output connection, and the data output register.

21. The multiple function system on a chip integrated circuit of claim 20, wherein the input/output selection module comprises:

a first control register operably coupled to store a multiplexer selection signal;

a second control register operably coupled to store an overwriting enable/disable signal;

a first multiplexer operably coupled to provide the outbound data signal to the input of the data output buffer when the multiplexer selection signal is in a first state and to provide the alternate output data signal to the input of the data output buffer when the multiplexer selection signal is in a second state; and

a second multiplexer operably coupled to provide an output enable signal to the data output buffer when the multiplexer selection signal is in a third state and to provide the overwriting enable/disable signal to the data output buffer when the multiplexer selection signal is in a fourth state.

22. The multiple function system on a chip integrated circuit of claim 21 further comprises:

the multiplexer signal being in the first state and the third state simultaneously, the first state and the fourth state simultaneously, the second state and the third state simultaneously, or the second state and the fourth state simultaneously.

23. The multiple function system on a chip integrated circuit of claim 16, wherein the at least one general purpose input/output (GPIO) interface module further comprises:

a first GPIO interface module operably coupled to first and second functional modules of the plurality of functional modules; and

a second GPIO interface module operably coupled to a third and fourth functional modules of the plurality of functional modules, wherein, when the configurable integrated circuit is in a third functional mode, a GPIO cell of the second GPIO interface module is operably coupled to a second corresponding pin such that the second corresponding pin functions as a digital input pin and when the configurable integrated circuit is in a second functional mode, the GPIO cell of the second GPIO interface module is operably coupled to the second corresponding pin such that the second corresponding pin functions as a digital output pin.